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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/056,224
Filing Date: January 22, 2002
Appellant(s): RAVICHANDRAN, HARI K.

Stephen A. Terrile, Reg. Number 32,946
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 10/28/2005 appealing from the Office action mailed 03/01/2005.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is incorrect.

The amendment after final rejection filed on 05/02/2005 has not been entered.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Prior Art of Record

Bunnell	U.S. Patent Number 5,564,015
Roeber	U.S. Patent Number 5,682,328
Levine	U.S. Patent Number 6,067,644
Razban	U.S. Patent Number 5,289,587

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell, U.S. Patent Number 5,564,015 and further in view of Roeber, et al, U.S. Patent Number 5,682,328.

Bunnell teaches a method for monitoring an execution of a program, the method comprising the steps of:

a. Obtaining a first instruction including a first address, (see col. 6, lines 54-56; a memory access instruction inherently includes an address);
b. Searching a first memory device for an entry associated with the first address, (see again, col. 6, lines 54-56);
c. When the entry in the first memory device does not exist, generating at least one probe signal, ("cache miss signal"), indicating a miss entry in the first memory device, (see col. 6, lines 58-61); and
d. Generating a temporal identifier signal that is associated with the cache miss signals, (note col. 4, lines 44-49, wherein a clock signal is associated with the cache miss signals).

Bunnell fails to teach that the probe signal and the temporal identifier signal are then stored in memory.

Roeber et al teaches a method for monitoring and analyzing system activity by recording event data along with time information associated with said event data, (see col. 3, lines 30-33 and col. 1, lines 33-35). Roeber et al, therefore, teaches the step of storing a temporal identifier signal and a probe signal, (or event data signal), in memory.

Bunnell and Roeber et al are analogous art because they are from the same field of endeavor, viz., monitoring the performance of a system by logging event data.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to include the step of storing the time and cache miss signals generated in Bunnell in the method taught by Bunnell, in view of the system disclosed in Roeber et al, which teaches the motivation for the storing of such information. Roeber et al teaches that time and event data should be stored in memory so that the record of events can be later analyzed to determine what actions took place at what times within the computer program being observed, (note col. 1, lines 35-39). One of ordinary skill in the art would have been motivated to store the time and cache miss signals generated in Bunnell, in view of Roeber et al, in order to enable future analysis of cache miss activity in the system.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell, in view of Roeber et al, as applied to claim 9 above, and further in view of Levine et al, (U.S. 6,067,644).

Regarding claim 11, Bunnell, in view of Roeber et al, as has already been shown, teaches the steps of:

- searching a first memory device for an entry associated with the first address, (step b),
- when the entry in the first memory device does not exist, generating at least one probe signal indicating a miss entry in the first memory device, (step c), and
- generating a temporal identifier signal that is associated with the probe signals, (step d).

Bunnell, in view of Roeber et al, fails to teach the steps of, after step (d):

- searching a second memory device for an entry associated with the first address,
- when the entry in the second memory device does not exist, generating at least one probe signal indicating a miss entry in the second memory device, and
- generating a temporal identifier signal that is associated with the probe signals.

Levine et al teaches a method of monitoring the execution of instructions in a program, including the steps of checking a second cache in the event that an entry in the first cache does not exist, (see col. 1, lines 57-61 and col. 2 lines 1-3).

Levine et al, Bunnell and Roeber et al are analogous art because they are all from the same field of endeavor, viz., monitoring and analyzing events in a computer system.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to include the steps of checking a second cache, in view of Levine et al, in the event that data is not located in the first cache, in the method taught by Bunnell in view of Roeber et al. Levine et al teaches that multiple caches can be used to improve system

performance. In a memory hierarchy scheme, data that is most frequently accessed is held in the smaller, and thus faster, memory of the first cache. Data that is less frequently accessed can then be held in a larger, and thus slower, memory of a second cache, and data that is infrequently accessed can be held in the largest, and thus slowest, system memory, (see col. 1, lines 64-67). Data that is more frequently accessed, therefore, is access more efficiently – improving performance. One of ordinary skill in the art would have been motivated to include a second cache in the method disclosed in Bunnell, in view of Roeber et al, in order to improve system performance. Moreover, one of ordinary skill in the art would have considered it obvious to perform the same steps in checking the second memory device as were performed in checking the first.

Claims 13 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell, and further in view of Roeber et al, and Levine et al.

Regarding claim 13, Bunnell teaches a method for monitoring an execution behavior of a program, comprising:

- Generating probe signals representative of memory access misses occurring in a processor, (see col. 6, lines 58-61);
- Receiving the probe signals and associating a temporal identifier signal with the probe signals, (note col. 4, lines 44-49, wherein a clock signal is associated with the cache miss signals); and
- Generating a first high-speed memory miss signal, (see col. 6, lines 58-61), a first high-speed memory miss count signal, (see col. 4, lines 49-53, and col. 9, lines 5-6), and a time stamp signal, (see col. 4, lines 44-45), the first high-speed memory

miss signal indicating a miss in a first high-speed memory, the first high-speed memory miss count signal representing a number of misses in the first high-speed memory, and the time stamp signal indicating when the first high-speed memory miss signal is active.

Bunnell fails to teach:

- Storing the temporal identifier signal and the probe signals; and
- Generating a second high-speed memory miss signal, a second high-speed memory miss count signal, and a time stamp signal, the second high-speed memory miss signal indicating a miss in a second high-speed memory, the second high-speed memory miss count signal representing a number of misses in the second high-speed memory, and the time stamp signal indicating when the second high-speed memory miss signal is active.

Roeber et al teaches a method for monitoring and analyzing system activity by recording event data along with time information associated with said event data, (see col. 3, lines 30-33 and col. 1, lines 33-35). Roeber et al, therefore, teaches the step of storing a temporal identifier signal and a probe signal, (or event data signal), in memory.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to include the step of storing the time and cache miss signals generated in Bunnell in the method taught by Bunnell, in view of the system disclosed in Roeber et al, which teaches the motivation for the storing of such information. Roeber et al teaches that time and event data should be stored in memory so that the record of events can be later

analyzed to determine what actions took place at what times within the computer program being observed, (note col. 1, lines 35-39). One of ordinary skill in the art would have been motivated to store the time and cache miss signals generated in Bunnell, in view of Roeber et al, in order to enable future analysis of cache miss activity in the system.

Levine et al teaches a method of monitoring the execution of instructions in a program, including the steps of checking a second cache in the event that an entry in the first cache does not exist, (see col. 1, lines 57-61 and col. 2 lines 1-3).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious to include the steps of checking a second cache, in view of Levine et al, in the event that data is not located in the first cache, in the method taught by Bunnell, and to subsequently utilize the teachings of Bunnell to analyze cache miss activity associated with second cache memory access attempts. Levine et al teaches that multiple caches can be used to improve system performance. In a memory hierarchy scheme, data that is most frequently accessed is held in the smaller, and thus faster, memory of the first cache. Data that is less frequently accessed can then be held in a larger, and thus slower, memory of a second cache, and data that is infrequently accessed can be held in the largest, and thus slowest, system memory, (see col. 1, lines 64-67). Data that is more frequently accessed, therefore, is accessed more efficiently – improving performance. One of ordinary skill in the art would have been motivated to include a second cache in the method disclosed in Bunnell, in view of Roeber et al, in order to improve system performance. Moreover, one of ordinary skill in the art would have considered it obvious to perform the same steps in

analyzing cache miss activity associated with the second memory device as were performed in analyzing cache miss activity associated with the first.

Regarding claim 14, see Bunnell, col. 6, lines 52-61. Bunnell teaches generating probe signals in response to a memory access miss signal when executing a specified instruction (i.e. a CPU 28 data request instruction).

Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell, in view of Roeber et al, as applied to claim 9 above, and further in view of Razban, (U.S. 5,289,587).

Bunnell, in view of Roeber et al, fails to teach that step (a) includes the step of incrementing a program counter with the first instruction, and fails to teach that step (c) includes the step of generating a second probe signal indicating a content of the program counter.

Razban teaches a method of monitoring system activity including the step of sending a signal indicating the content of a program counter. Razban teaches that content of the program counter is provided upon execution of each instruction, (see col. 4, lines 35-38), and that the program counter value is incremented when a new instruction is initiated, (see col. 4, lines 31-34). Razban also teaches that the program counter value is sent in the event of a cache miss, (note col. 4, lines 18-22 and 53-61).

Razban, Bunnell and Roeber et al are analogous art because they are all from the same field of endeavor, viz., methods for monitoring system progress or performance.

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious, in view of Razban, to increment a program counter when initiating an instruction, and include a signal containing the program counter value in the event of a cache miss, in the method disclosed in Bunnell in view of Roeber et al. Razban teaches that, when monitoring a system for bugs, one of the most important elements of information to be traced is the value of the program counter, (see col. 1, lines 30-35). This value allows the monitoring system to follow the sequence of instruction execution in the program operating the system, to better be able to identify a bug in the process with a specific instruction, (see col. 1, lines 39-42). One of ordinary skill in the art would, therefore, have been motivated to include a program counter in the method of Bunnell, in view of Roeber et al, and the steps of incrementing the program counter with the initiation of an instruction and sending the program counter value along with the cache interrupt signal, in order to enable a monitoring system to identify the cache interrupt event with the specific instruction.

Claim 12 is rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell, in view of Roeber et al, as applied to claim 9 above, and further in view of Mahalingaiah et al, (U.S. 5,933,626).

Bunnell, in view of Roeber et al, fails to teach a step of, before step (b):

- searching an address storage device for an entry associated with the first address,
- when the entry in the address storage device does not exist, generating at least one probe signal indicating a miss entry in the address storage memory device, and
- generating a temporal identifier signal that is associated with the probe signal.

Mahalingaiah et al teaches a method for tracing microprocessor instructions that comprises searching a TLB for an entry associated with an address, and responding to a TLB miss event, (see col. 16, lines 29-29). The TLB is an address storage device that stores the virtual-to-physical translations of the most recently accessed data blocks.

Mahalingaiah et al, Bunnell, and Roeber et al are analogous art because they all are from the same field of endeavor, viz., methods for monitoring instructions and processes in a computer system.

At the time of applicant's invention, one of ordinary skill in the art, as has already been shown, would have considered it obvious, in view of Bunnell and Roeber et al, to search a memory device for an entry associated with an address, and generate time and cache miss signals if the entry does not exist. One of ordinary skill would have also considered it obvious to use an address storage device, as taught in Mahalingaiah et al, in the method disclosed in Bunnell, in view of Roeber et al. The TLB disclosed in Mahalingaiah et al, provides a more efficient means of storing those addresses that were most recently accessed. If the data associated with an address is very large, efficiency can be improved in a caching system by storing only a new physical address location, in a TLB, that is associated with the most frequently or recently accessed data. Replacing address entries in the TLB would require less processing power than replacing data entries in a cache. One of ordinary skill in the art would, therefore, have been motivated to include the steps of searching an address storage device for an entry associated with a first address, before searching a first memory device, in order to improve efficiency in the system. Moreover, one

of ordinary skill would have considered it obvious to check the address storage device with the same method used to check the first memory device.

Claims 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell in view of Roeber et al and Levine et al, (hereinafter referred to as Bunnell-Roeber-Levine), as applied to claim 13 above, and further in view of Razban and Mahalingaiah et al.

Regarding claims 15 and 16, Bunnell-Roeber-Levine teaches:

- Generating probe signals recording a cache miss when executing a specified instruction, (see Bunnell, col. 6, lines 52-61); and
- Generating an identification signal indicating a miss in the cache, (see Bunnell, col. 6, lines 58-61), a cache miss count signal representing an accumulative count of cache misses, (see Bunnell, col. 4, lines 49-53, and col. 9, lines 5-6), and a time stamp signal when the cache miss signal is activated, (see col. 4, lines 44-45).

Bunnell-Roeber-Levine fails to teach:

- Generating a program counter signal; and
- Generating those signals indicated above in response to a TLB miss rather than a cache miss.

Razban teaches a method of monitoring system activity including the step of sending a signal indicating the content of a program counter. Razban teaches that content of the program counter is provided upon execution of each instruction, (see col. 4, lines 35-38), and that the program counter value is incremented when a new instruction is initiated, (see

col. 4, lines 31-34). Razban also teaches that the program counter value is sent in the event of a cache miss, (note col. 4, lines 18-22 and 53-61).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious, in view of Razban, to increment a program counter when initiating an instruction, and include a signal containing the program counter value in the event of a cache miss, in the method disclosed in Bunnell-Roeber-Levine. Razban teaches that, when monitoring a system for bugs, one of the most important elements of information to be traced is the value of the program counter, (see col. 1, lines 30-35). This value allows the monitoring system to follow the sequence of instruction execution in the program operating the system, to better be able to identify a bug in the process with a specific instruction, (see col. 1, lines 39-42). One of ordinary skill in the art would, therefore, have been motivated to include a program counter in the method of Bunnell-Roeber-Levine, and the steps of incrementing the program counter with the initiation of an instruction and sending the program counter value along with the cache miss signal, in order to enable a monitoring system to identify the cache miss event with the specific instruction.

Mahalingaiah et al teaches a method for tracing microprocessor instructions that comprises searching a TLB for an entry associated with an address, and responding to a TLB miss event, (see col. 16, lines 29-29). The TLB is an address storage device that stores the virtual-to-physical translations of the most recently accessed data blocks.

At the time of applicant's invention, one of ordinary skill in the art, as has already been shown, would have considered it obvious, in view of Bunnell-Roeber-Levine, and further in

view of Razban, to search a memory device for an entry associated with an address, and generate program counter, time stamp, miss count, and cache miss signals if the entry does not exist. One of ordinary skill would have also considered it obvious to use an address storage device, as taught in Mahalingaiah et al, in the method disclosed in Bunnell-Roeber-Levine, in view of Razban. The TLB disclosed in Mahalingaiah et al, provides a more efficient means of storing those addresses that were most recently accessed. If the data associated with an address is very large, efficiency can be improved in a caching system by storing only a new physical address location, in a TLB, that is associated with the most frequently or recently accessed data. Replacing address entries in the TLB would require less processing power than replacing data entries in a cache. One of ordinary skill in the art would, therefore, have been motivated to include the steps of searching TLB for an entry associated with a first address, before searching a first memory device, in order to improve efficiency in the system. Moreover, one of ordinary skill would have considered it obvious to analyze TLB misses using the same method used to analyze cache misses in Bunnell-Roeber-Levine, in view of Razban.

Regarding claim 17, see Bunnell, col. 4, lines 49-53, and note the discussion above relating cache miss analysis to TLB miss analysis.

Claims 18 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bunnell in view of Roeber et al and Levine et al, (hereinafter referred to as Bunnell-Roeber-Levine), as applied to claim 13 above, and further in view of Razban.

Regarding claim 18, Bunnell-Roeber-Levine teaches the method of claim 13, wherein:

- The program executes on a processor, (see Bunnell, col. 6, lines 40-51);
- The processor includes a first high-speed memory, the first high-speed memory generating a first high-speed memory miss signal, (see Bunnell, col. 6, lines 52-61); and
- A probe logic unit, (see Bunnell, col. 3, lines 57-58), generates a first high-speed memory miss signal indicating a miss in the first high-speed memory, (see Bunnell, col. 6, lines 58-61), a first high-speed memory miss count signal representing a number of misses in the first high-speed memory, (see Bunnell, col. 4, lines 49-53), and a time stamp signal when the first high-speed memory miss signal is activated, (see col. 4, lines 44-45).

Bunnell-Roeber-Levine fails to teach that the processor includes a program counter, (though, inclusion of a program counter with a processor would be considered obvious to one of ordinary skill in the art), and that the probe logic unit generates a program counter signal.

Razban teaches a method of monitoring system activity including the step of sending a signal indicating the content of a program counter. Razban teaches that content of the program counter is provided upon execution of each instruction, (see col. 4, lines 35-38), and that the program counter value is incremented when a new instruction is initiated, (see col. 4, lines 31-34). Razban also teaches that the program counter value is sent in the event of a cache miss, (note col. 4, lines 18-22 and 53-61).

At the time of applicant's invention, one of ordinary skill in the art would have considered it obvious, in view of Razban, to increment a program counter, included in a processor, when initiating an instruction, and include a signal containing the program counter value in the event of a cache miss, in the method disclosed in Bunnell-Roeber-Levine. Razban teaches that, when monitoring a system for bugs, one of the most important elements of information to be traced is the value of the program counter, (see col. 1, lines 30-35). This value allows the monitoring system to follow the sequence of instruction execution in the program operating the system, to better be able to identify a bug in the process with a specific instruction, (see col. 1, lines 39-42). One of ordinary skill in the art would, therefore, have been motivated to include a program counter in the method of Bunnell-Roeber-Levine, and the steps of incrementing the program counter with the initiation of an instruction and sending the program counter value along with the cache miss signal, in order to enable a monitoring system to identify the cache miss event with the specific instruction.

Regarding claim 19, see Bunnell, col. 4, lines 49-53.

(10) Response to Argument

Regarding the arguments supplied in the appeal brief for claim 9: (See pages 3-5 of the brief). The applicant argues that the prior art combination of Bunnell and Roeber does not individually or jointly teach or suggest "a method for monitoring an execution of a program which includes when the entry in the first memory device does not exist, generating at least one probe signal indicating a miss entry in the first memory device; generating at least one probe signal indicating a miss entry in the first memory device; generating a temporal identifier signal that is **associated with the probe signal**; and **storing the temporal identifier signal and the probe**

signals in memory," (bottom of page 4, top of page 5 of the brief; emphasis added by the applicant). The examiner respectfully disagrees. The examiner contends that the prior art of record, Bunnell and Roeber, do teach the claimed invention. Bunnell discloses a "miss cache signal" (lines 58-61 of Column 6), which the examiner equates to the claimed "one probe signal indicating a miss entry in the first memory device," as recited in the third limitation of claim 9. The examiner further contends that Bunnell disclose a clock signal that is generated by the system clock the measures a time interval associated with the miss cache signal initiation. (Lines 62-67 of Column 6 and Lines 1-5 of Column 7). The examiner equates this clock signal as the "temporal identifier that is associated with the probe signals" (limitation 4 of claim 9). Finally, the examiner contends that Bunnell also discloses a time register that stores the timer for the time interval of the miss cache signal. (Lines 39-60 of Column 7). The examiner acknowledges that the previous paragraphs have not been presented before in any action however, the examiner reminds applicant of the responsibility to read and consider the entirety of the reference for all that it discloses.

Bunnell fails to disclose storing the miss cache signal. However, Roeber teaches of a system that stores event information in a record. One of ordinary skill would have been inclined to combine that art. (Previously stated above). Therefore, Roeber discloses storing the "probe signal" (limitation 5 of claim 9) in memory. Thereby, Bunnell and Roeber taken together, in the examiner opinion, disclose all of the claimed limitation.

Regarding the arguments supplied in the appeal brief for claim 13: (See pages 3-5 of the brief). The applicant argues that the prior art combination of Bunnell and Roeber does not individually or jointly teach or suggest "a method for monitoring an execution of a program which includes when the entry in the first memory device does not exist, generating at least one probe

signal indicating a miss entry in the first memory device; generating at least one probe signal indicating a miss entry in the first memory device; generating a temporal identifier signal that is **associated with the probe signa**l; and **storing the temporal identifier signal and the probe signals in memory**," (bottom of page 4, top of page 5 of the brief; emphasis added by the applicant). The examiner respectfully disagrees. The examiner contends that the prior art of record, Bunnell and Roeber, do teach the claimed invention. Bunnell discloses a "miss cache signal" (lines 58-61 of Column 6), which the examiner equates to the claimed "one probe signal indicating a miss entry in the first memory device," as recited in the third limitation of claim 9. The examiner further contends that Bunnell disclose a clock signal that is generated by the system clock the measures a time interval associated with the miss cache signal initiation. (Lines 62-67 of Column 6 and Lines 1-5 of Column 7). The examiner equates this clock signal as the "temporal identifier that is associated with the probe signals." Finally, the examiner contends that Bunnell also discloses a time register that stores the timer for the time interval of the miss cache signal. (Lines 39-60 of Column 7). The examiner acknowledges that the previous paragraphs have not been presented before in any action however, the examiner reminds applicant of the responsibility to read and consider the entirety of the reference for all that it discloses.

Bunnell fails to disclose storing the miss cache signal. However, Roeber teaches of a system that stores event information in a record. One of ordinary skill would have been inclined to combine that art. (Previously stated above). Therefore, Roeber discloses storing the "probe signal" in memory. Thereby, Bunnell and Roeber taken together, in the examiner opinion, disclose all of the claimed limitation.

Regarding the arguments supplied in the appeal brief for claim 13: (See pages 6 of the brief). The applicant argues that the prior art combination of Bunnell, Roeber, and Levine does

not individually or jointly teach or suggest "generating a second high-speed memory miss signal, **a second high-speed memory miss count signal** and a time stamp signal, the second high-speed memory miss signal indicating a miss in a second high-speed memory, **the second high-speed memory miss count signal representing a number of misses in the second high-speed memory, and the time stamp signal indication when the second high-speed memory miss signal is active**." (page 6 of the brief; emphasis added by the applicant). The applicant goes on to argue, "it does not follow that it would have been obvious to analyze cache miss activity for multilevel or multiple caches as claimed merely because Levine discloses two levels of cache memory. The examiner respectfully disagrees. First, Bunnell disclose a need to check a second level of memory upon receiving a cache miss signal for a first memory. (Lines 55-58 of Column 6). Levine answers that need and includes checking of a second level of "staging area memory" (the examiner read this as a form of cache memory), before going to main system memory. Thereby, one of ordinary skill in the art would concluded that a first miss signal would be needed to check the first cache memory, and then a second missed cache signal would be need for the second memory, before attempting main system memory. Levine even goes so far as to say "An access in which the required datum is 'missing' from the cache is called 'cache miss.' The ratio of cache misses to cache access is called the 'cache miss ratio.' Accompanying the cache miss ratio is the amount of time required to obtain the missing datum. The hierarchical cache levels are accessed sequentially. The first caches are usually the fastest but also the least capacious. Each subsequent cache is larger in capacity but slower to access." (Lines 8-15 of Column 2). Thereby, in the examiners opinion, Levine discloses a system that has multiple cache levels which require multiple cache miss signals that equates to the claimed second memory device with a probe signal. Levine also discloses the need to maintain quick access in higher level of hierarchical cache levels so as to maintain a faster rate

of memory return. (Lines 12-15 of Column 2). The examiner equates this hierarchical cache levels as high-speed first and second memory levels. Therefore, Levin, in combination with Bunnell and Roeber provide "generating a second high-speed memory miss signal, a second high-speed memory miss count signal and a time stamp signal, the second high-speed memory miss signal indicating a miss in a second high-speed memory, the second high-speed memory miss count signal representing a number of misses in the second high-speed memory, and the time stamp signal indication when the second high-speed memory miss signal is active," as stated in the claim 13. Thereby, Bunnell, Levine and Roeber taken together, in the examiner opinion, disclose all of the claimed limitation.

Regarding the arguments supplied in the appeal brief for claim 11: (See pages 6 of the brief). The applicant argues that the prior art combination of Bunnell, Roeber, and Levine does not individually or jointly teach or suggest "a second memory device for an entry associated with the first address, when the entry in the second memory device does not exist **generating at least one probe signal indication a miss entry in the second memory device**, and generating a temporal identifier signal that is associated with the probe signal. (page 6 of the brief; emphasis added by the applicant). The applicant goes on to argue, "it does not follow that it would have been obvious to analyze cache miss activity for multilevel or multiple caches as claimed merely because Levine discloses two levels of cache memory. The examiner respectfully disagrees. First, Bunnell disclose a need to check a second level of memory upon receiving a cache miss signal for a first memory. (Lines 55-58 of Column 6). Levine answers that need and includes checking of a second level of "staging area memory" (the examiner read this as a form of cache memory), before going to main system memory. Thereby, one of ordinary skill in the art would concluded that a first miss signal would be needed to check the

first cache memory, and then a second missed cache signal would be need for the second memory, before attempting main system memory. Levine even goes so far as to say "An access in which the required datum is 'missing' from the cache is called 'cache miss.' The ratio of cache misses to cache access is called the 'cache miss ratio.' Accompanying the cache miss ratio is the amount of time required to obtain the missing datum. The hierarchical cache levels are accessed sequentially. The first caches are usually the fastest but also the least capacious. Each subsequent cache is larger in capacity but slower to access." (Lines 8-15 of Column 2). Thereby, in the examiners opinion, Levine discloses a system that has multiple cache levels which require multiple cache miss signals that equates to the claimed second memory device with a probe signal. Therefore, Levin, in combination with Bunnell and Roeber provide "a second memory device for an entry associated with the first address, when the entry in the second memory device does not exist generating at least one probe signal indication a miss entry in the second memory device, and generating a temporal identifier signal that is associated with the probe signal," as stated in the claim 11. Thereby, Bunnell, Levine and Roeber taken together, in the examiner opinion, disclose all of the claimed limitation.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

tmb - 03/17/2006

Conferees:

SCOTT BADERMAN
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for
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